Errata for MIPS R4000/R4400 Microprocessor User's Manual, 2nd. Edition

This errata supplements the "MIPS R4000/R4400 User's Manual, 2nd Edition" by Joe Heinrich

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At the end of the section titled SyncIn/SyncOut, add the following:
The delay allowed between the SyncOut and SyncIn must be no more than [1/2*MasterClock cycle - 2nS]

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In Table 12-3, for Page Attribute "Exclusive" the Processor Configuration should be only R4000MC (remove "R4000SC)

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At the end of the sentence in the ninth line: "Figures 12-24 through 12-27 illustrate .... below.
Add the following sentence: "All the waveforms are shown with zero delay from the SClock's rising edge; i.e. outputs are driven by the processor at the corresponding rising edge and inputs are driven by the external logic at the corresponding rising edge of the SClock.
Also at the end of the paragraph describing Figure 12-24: "Figure 12-24 illustrates .... WrRdy*.
Add the following sentence: "In this example, the WrRdy* must be deasserted in cycle 5 (sampled by the processor at the rising edge of cycle 6) to delay the issue cycle that would have occurred in cycle 7. Assertion of WrRdy* in cycle 8 (sampled by the processor at the rising edge of cycle 9) will cause the Write Request to be issued in cycle 10.