Output Buffer Δi/Δt Control Mechanism

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The speed of the R4000 output drivers is controlled by a negative feedback loop that insures the drive-off times are only as fast as necessary to meet the system requirement for single cycle transfers. This guarantees the minimum ground bounce from L*(Δi/Δt) of the switching buffers, consistent with the system timing requirements.

D.1 Mode Bits

Four bits are used to control the pull-up and pull-down delays. These bits are initially set to the values in the mode bits **InitN(3:0)** for pull-up and **InitP(3:0)** for pull-down. If the Δi/Δt control mechanism is enabled, it is recommended to load the mode bits **InitP(3:0)** and **InitN(3:0)** to the values which provide the slowest slew rate.

Under normal conditions, the Δi/Δt control mechanism is enabled to compensate the output buffer delay for any changes in the temperature or power supply voltage. The **EnblDPLL** mode bit is set for this mode of operation.

For situations where the jitter associated with the operation of the Δi/Δt control mechanism cannot be tolerated and where the variation in temperature and supply voltage after **ColdReset*** is expected to be small, the Δi/Δt control mechanism can be instructed to lock during **ColdReset*** and thereafter retain its control values. The **EnblDPLLR** mode bit is set and **EnblDPLL** is cleared for this mode of operation.

In addition, if both the **EnblDPLL** and **EnblDPLLR** mode bits are cleared, the speed of the output buffers are set by the **InitP(3:0)** and **InitN(3:0)** mode bits.

D.2 Delay Times

Currently, delays of 0.5T, 0.75T, and T are supported, corresponding to the **Drv0_50**, **Drv0_75**, and **Drv1_00** mode bits, where T is the **MasterClock** period. For example, in **Drv0_75** mode, the entire signal transmission path including the clock-to-Q, output buffer drive time, board flight time, input buffer delay, and setup time will be traversed in 0.75 * the **MasterClock** period, plus or minus the jitter due to the Δi/Δt control mechanism.

All output drivers on the R4000, with the exception of the clock drivers, are controlled by the Δi/Δt control mechanism. The delay due to the output buffer drive time component of the **SCAddr(17:0)**, **SCOEB**, **SCWRB**, **SCDCSB**, and **SCTCSB** pins is approximately 66% of the delay of drivers of the other pins.

By measuring the transmission line delay of the trace that connects the R4000 **IO_Out** and **IO_In** pins, the R4000 determines the worst case propagation delay from an R4000 output driver to a receiving device. This representative trace must have one and a half times the length and approximately the same capacitive loading as the worst case trace on any R4000 output.

The designer determines the trace characteristics by:

- measuring the longest path from an R4000 output driver to a receiving device, *L*
- calculating the maximum capacitive loading on any signal pin, *C*
- connecting an incident-wave trace of length *L* with a capacitive loading of *C* between the **IO_In** and **IO_Out** pins of the R4000
- connecting a reflected wave trace of length *L*/2 to the **IO_In** pin of the R4000.

An R4000 with appropriate traces connected to the **IO_In** and **IO_Out** pins is illustrated in Figure D-1.

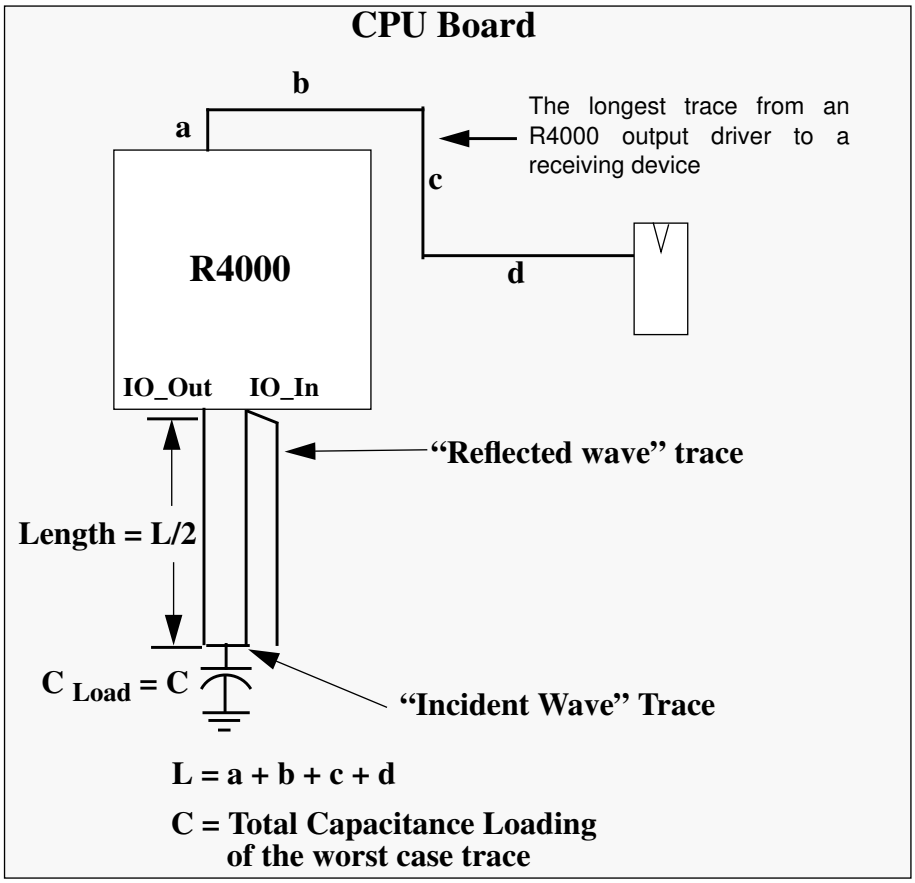

Figure D-1 O_In/IO_Out Board Trace