MIPS RISC ARCHITECTURE
outline

INTRODUCTION

INSTRUCTION SET

PIPELINE EFFICIENCY

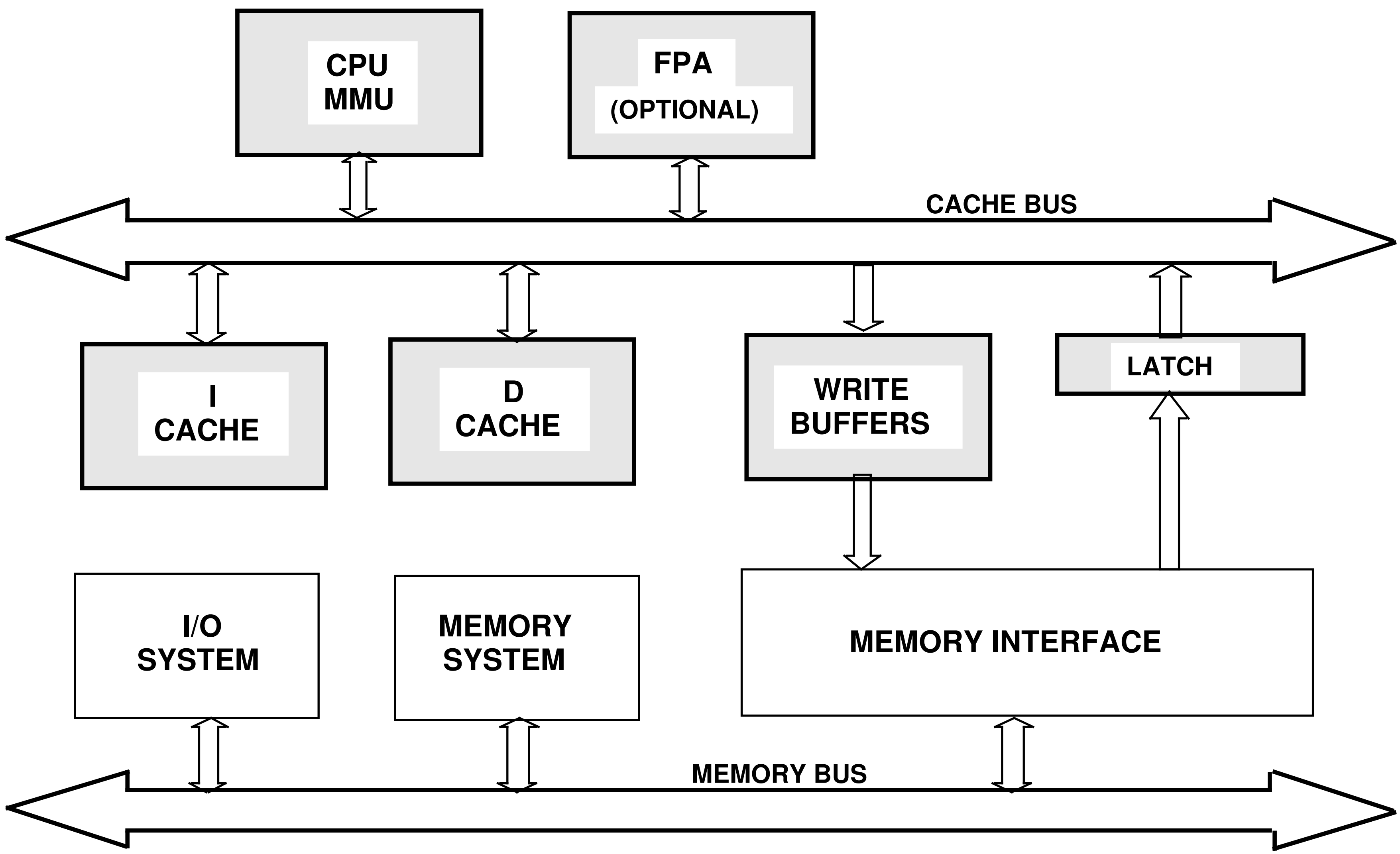
MEMORY MANAGEMENT

CACHE MEMORY

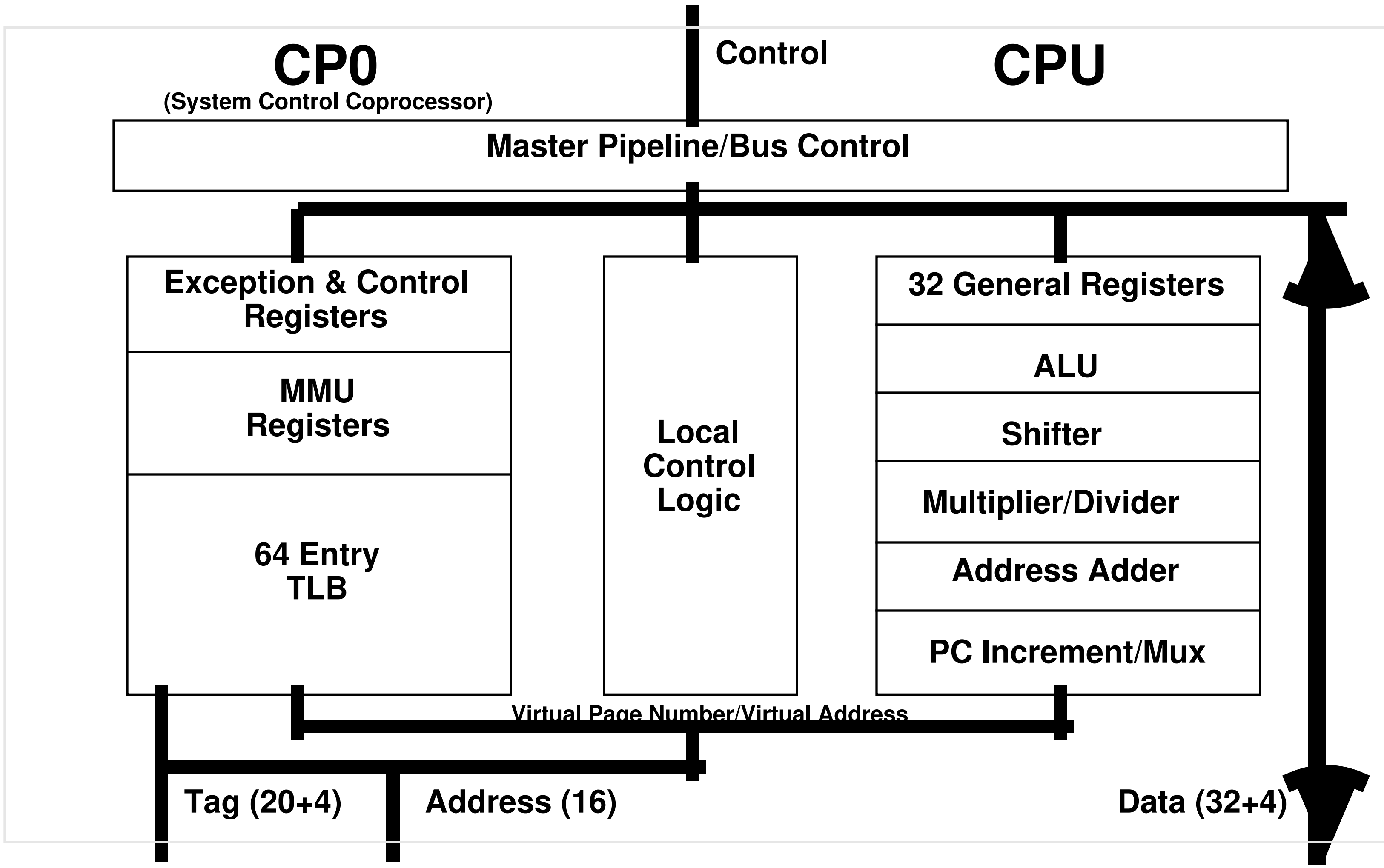
EXCEPTION HANDLING

MULTIPROCESSORS

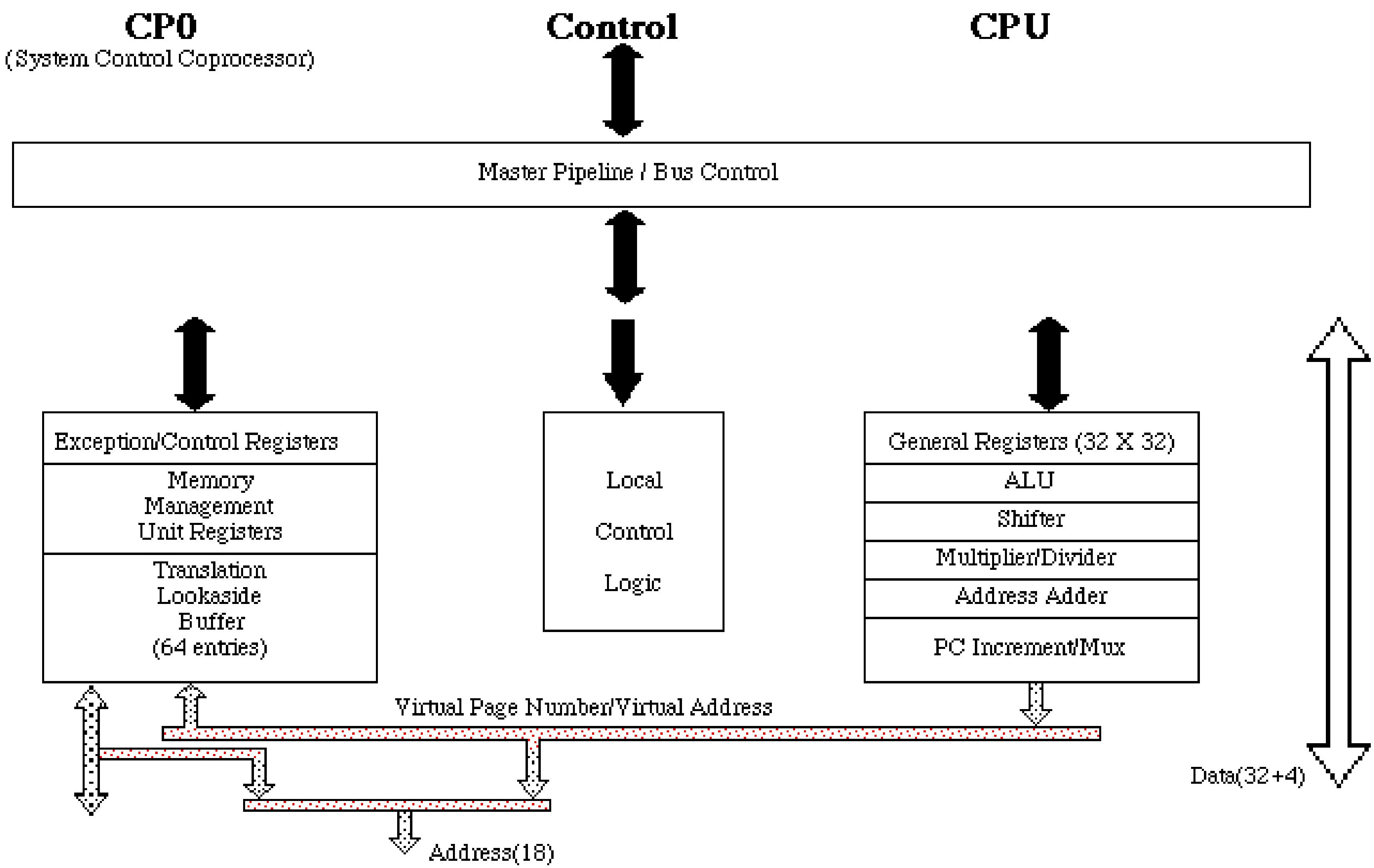
SYSTEM BLOCK DIAGRAM



R3000 BLOCK DIAGRAM

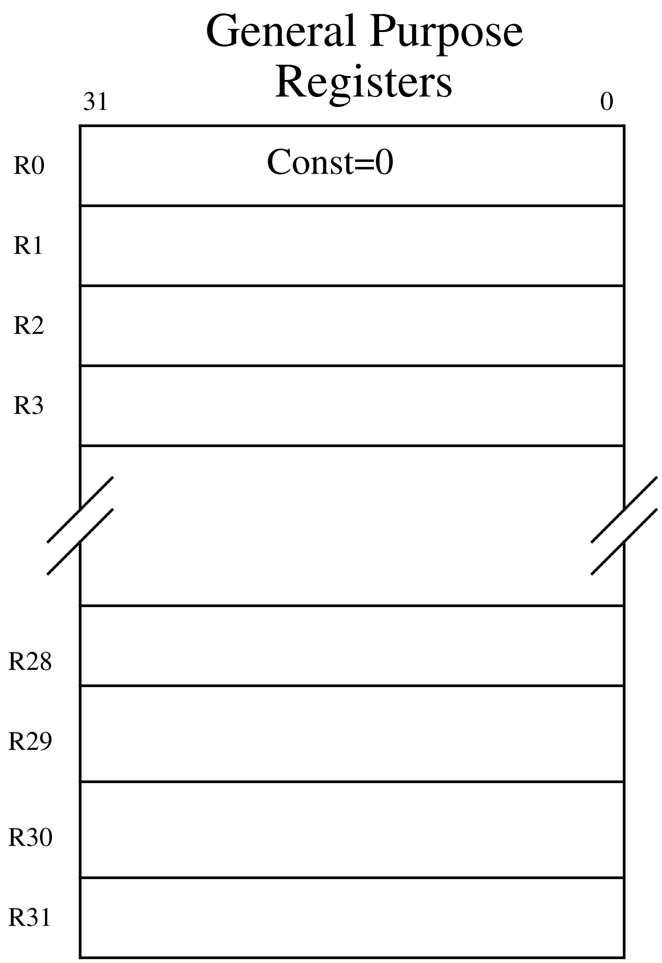


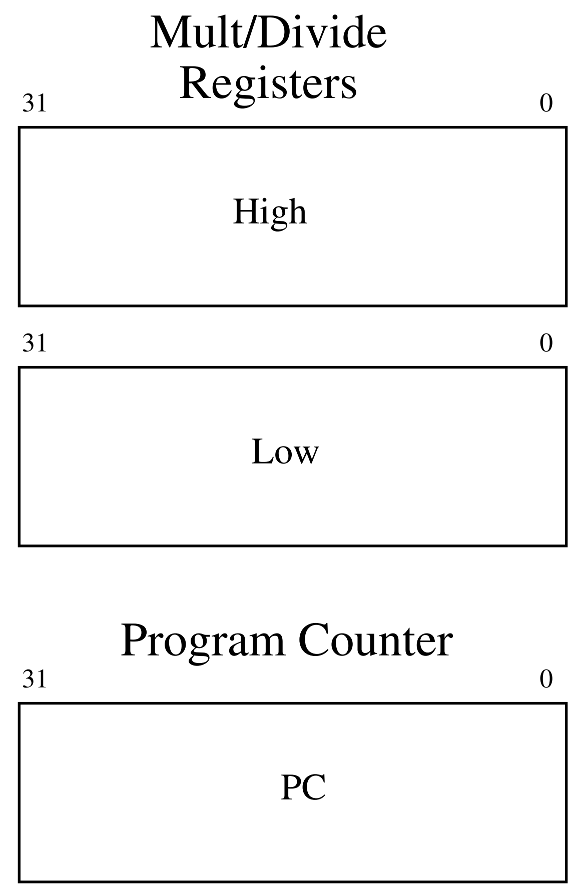
LR3000 CPU BLOCK DIAGRAM



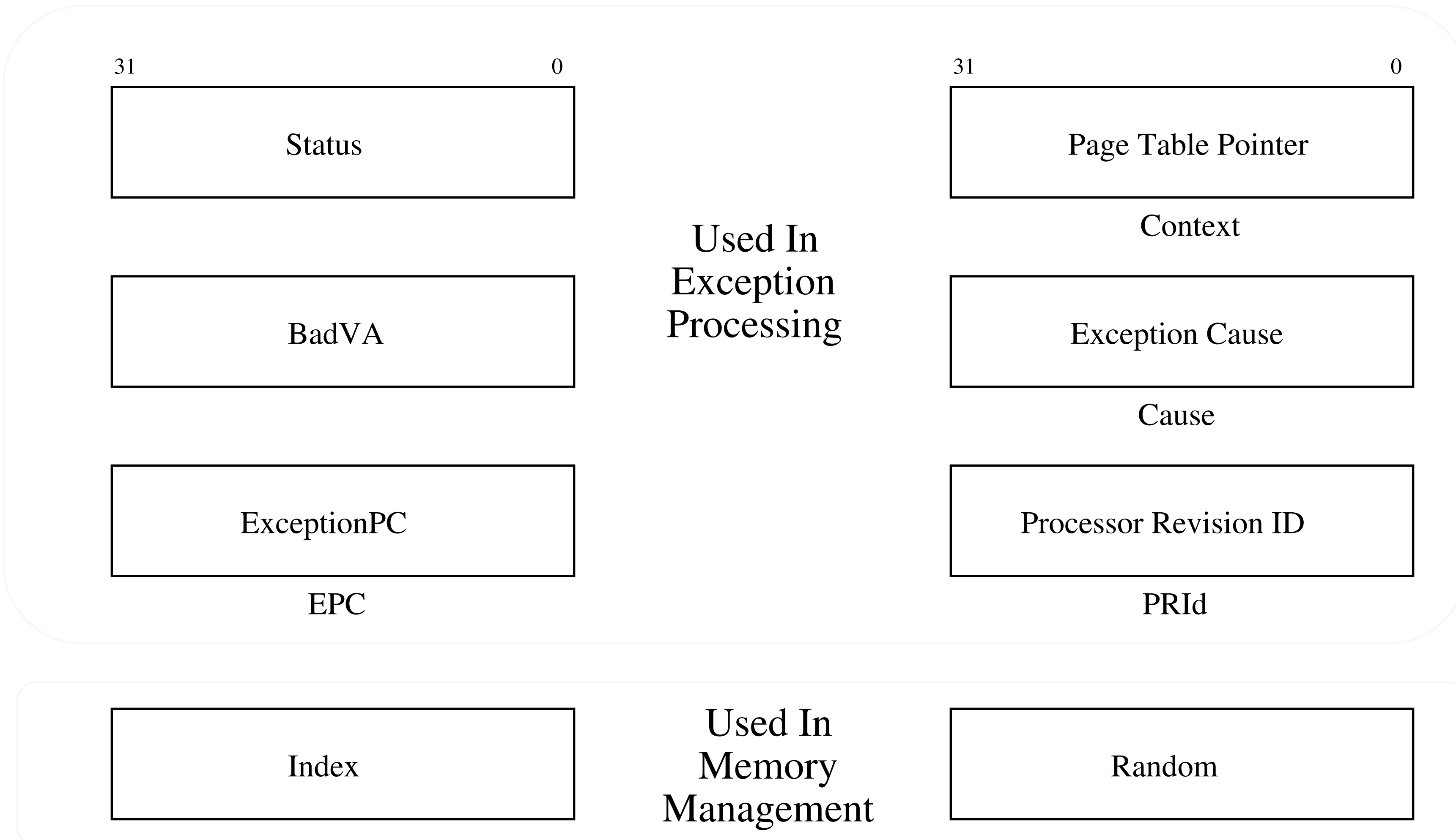
- **LR3000 Supports Up To 4 Coprocessors**

LR3000 CPU REGISTERS





LR3000 CONTROL REGISTERS (CP0)



MMU REGISTERS (CP0)